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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,256	10/12/2001	Krishnaswamy Ramkumar	8229-014-27	8851

7590 08/05/2002

Supervisor, Patent Prosecution Services
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EXAMINER
HOGANS, DAVID L

ART UNIT	PAPER NUMBER
2813	5

DATE MAILED: 08/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No. 09/975,256	Applicant(s) RAMKUMAR ET AL.	
	Examiner David L. Hogans	Art Unit 2813	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al.

Claim 1-6 and 19

Yu et al. teaches a method for forming a nitrided gate oxide layer on a semiconductor substrate by annealing the substrate with NO at 600-800 °C and $1x10^{-6}$ torr. (See column 5 lines 10-20)

Yu et al. fails to explicitly teach wherein the oxide layer is formed preceding the step of nitriding the oxide layer.

However, Yu et al., in column 5 lines 10-20, teaches a layer (18) that is an oxide with a heavy concentration of nitride. Although Yu et al. does not teach the formation of the oxide layer preceding the NO exposure, the simultaneous formation of the nitrided gate oxide layer by Yu et al. is seen as equivalent. Furthermore, Applicants

specification contains no disclosure of either the critical nature of forming the oxide layer before NO nitridation or any unexpected results arising therefrom.

It would have been obvious to one or ordinary skill in the art to modify Yu et al. by forming the oxide layer before NO nitridation. Yu's et al. modification is obvious because simultaneous formation of the nitrided gate oxide layer is seen as equivalent to forming the oxide layer before NO nitridation.

Claim 16

Incorporating all arguments of Claim 1 and noting that since Yu et al. performs the nitrided oxide layer formation under the same process conditions (i.e. – below 800 °C and below 1 atmosphere) as Applicant's claim, the oxide layer will have at least 1.5 at.% nitrogen incorporated into the oxide layer during the nitriding step.

3. Claims 7, 8, 17, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al. in view of Microchip Fabrication to Van Zant.

Claims 7 and 20

Yu et al. in column 5 lines 27-40, teaches a reoxidation step after the formation of the nitrided oxide layer (18) by the introduction of a nitrided oxide gas. Furthermore, Van Zant in pages 503 and 513, teaches the formation of a ONO (oxide-nitride-oxide) layer in capacitors and MOSFET's due to its lower dielectric constant. Therefore, it

would have been obvious to one of ordinary skill in the art to construct a ONO layer in a MOSFET structure.

Claims 8 and 22

Yu et al. discloses the claimed method except for the explicit formation of a gate electrode. However, Yu et al., in column 4 lines 13-15 teaches the above process for the formation of a gate oxide layer which inherently implies this application to a gate electrode. Additionally, Van Zant in pages 188-189, discloses that it is known within the art to provide a gate electrode over a nitrided oxide film. It would have been obvious to one of ordinary skill in the art to a gate structure formed over a nitrided oxide layer.

Claim 17

Incorporating all arguments of Claim 1 and noting that Yu et al. fails to explicitly teach forming the oxide layer by a dry oxide method.

However, Van Zant, on page 160, graphically shows the deposition of silicon dioxide by dry oxide per the parameters of time, thickness and temperature. Examiner notes that it is well known within the art to form an oxide layer over a silicon substrate to act as an insulator. (See Van Zant page 156) Therefore, it would have been obvious to one of ordinary skill in the art to modify Yu et al. in view of Van Zant's teachings of a silicon dioxide layer by a dry oxide method at 800 °C.

4. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al. in view of 5,766,994 to Tseng in view of Microchip Fabrication to Van Zant.

Incorporating all arguments of Claim 8 and noting that Yu et al. fails to explicitly teach wherein the gate electrode layer is comprised by polysilicon and a layer of tungsten or tungsten silicide.

However, Tseng, in columns 4 and 5 lines 64-05, teaches the formation of a polysilicon layer that is then topped with a tungsten silicide layer. Furthermore, Van Zant teaches that one would top the polysilicon layer with a refractory metal silicide to provide a low contact resistance. (See page 514)

It would have been obvious to one of ordinary skill in the art to modify Yu et al. in view of Tseng's and Van Zant's teachings of a tungsten silicide layer formed over the polysilicon gate. Yu's et al. modification via Tseng's and Van Zant's teachings is obvious because one would top the polysilicon layer with a refractory metal silicide to provide a low contact resistance.

5. Claims 11, 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al. in view of 5,766,994 to Tseng in view of Microchip Fabrication to Van Zant further in view of Applicants own specification.

Incorporating all arguments of Claims 8 and 19 and noting that Yu et al. and Tseng fail to teach doping the gate electrode with boron.

However, Applicants specification, pages 1 and 2 lines 15-22, teach the boron doping of gate electrodes as well known within the art. Therefore, it would have been obvious to one of ordinary skill in the art to boron dope the gate electrode in view of Applicant's disclosure.

6. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al. in view of 6,399,520 to Kawakami et al. in view of Microchip Fabrication to Van Zant.

Incorporating all arguments of Claim 1 and noting that Yu et al. fails to explicitly teach forming an SiO_2 layer or an oxide layer that has a thickness of about 15 angstroms.

However, Kawakami et al., in column 16 lines 20-30 and 40-50, teaches forming an SiO_2 layer by a thermal oxidation step at a thickness of 20 angstroms. Examiner notes that it is well known within the art to form an oxide layer over a silicon substrate to act as an insulator. (See Van Zant page 156) Although Kawakami et al. does not explicitly teach a thickness of 15 angstroms; without supporting evidence within the

Applicant's specification showing criticality of this dimension, Kawakami's et al. dimension of 20 angstroms is deemed equivalent. Finally, Examiner notes that it is well known within the art to make the gate oxide as thin as possible so as to make the device faster and lower threshold voltage. (See Van Zant page 513)

It would have been obvious to one of ordinary skill in the art to modify Yu et al. in view of Kawakami et al. and Van Zant's teachings of forming an SiO_2 layer by a thermal oxidation step at a thickness of 20 angstroms. Yu et al. modification via Kawakami et al. and Van Zant's teachings is obvious because it is well known within the art to form an oxide layer over a silicon substrate and it is well known with in the art to make the gate oxide as thin as possible so as to make the device faster and lower threshold voltage.

7. Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over 6,180,543 to Yu et al. in view of Microchip Fabrication to Van Zant.

Yu et al. discloses the claimed method except for the explicit formation of a gate electrode over a oxidized nitrided gate oxide layer. However, Yu et al., in column 4 lines 13-15 teaches the above process for the formation of a gate oxide layer which inherently implies this application to a gate electrode. Additionally, Van Zant on page 189, discloses that it is known within the art to provide a gate electrode over a oxidized

nitrided oxide film. It would have been obvious to one of ordinary skill in the art to a gate structure formed over a nitrided oxide layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

C. Chaudhari

Chandra Chaudhari
Primary Patent Examiner

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August 1, 2002